REMARKS

Favorable reconsideration of this application in light of the following discussion is respectfully requested.

Claims 1-7 and 12-20 are presently active in this case. The present Amendment amends Claims 1-2 and 17 without introducing any new matter and cancels Claims 8-11.

Claims 1-11, 14, 17-18 and 20 were rejected under 35 U.S.C. §103(a) as unpatentable over Butt (U.S. Patent No. 4,524,238) in view of Stobbs (U.S. Publication No. 2004/0150091). Claims 12-13 and 19 were rejected under 35 U.S.C. §103(a) as unpatentable over Butt, Stobbs and further in view of Hirai (U.S. Publication No. 2002/0131296). Claims 15-16 were rejected under 35 U.S.C. §103(a) as unpatentable over Stobbs.

In order to clarify Applicant's invention, independent Claims 1, 2 and 17 are amended to recite features regarding a lead frame including a die pad, an inner lead portion and an outer lead portion. These features find non-limiting support in the disclosure as originally filed, for example from page 11, line 12 to page 12, line 12 and in corresponding Figures 2, 5-6. Consequently, Claims 8-11 are cancelled as being conflicting with the new features of independent Claim 1.

In response to the rejection of Claims 1-11, 14, 17-18 and 20 under 35 U.S.C. §103(a) over Butt and Stobbs, Claims 12-13 and 19 under 35 U.S.C. §103(a) over Butt, Stobbs and Hirai, and Claims 15-16 under 35 U.S.C. §103(a) over Stobbs, and in view of the above-noted amendments, Applicant respectfully requests reconsideration of these rejections and traverses the rejections, as discussed next.

Briefly recapitulating, Applicant's invention, as recited in independent Claim 1, relates to a semiconductor device including: a semiconductor chip including a magnetic element; an enclosure which seals the semiconductor chip and has a base material and a cap material joined together via a sealing material; substantially spherical magnetic substance

particles which are interspersed in the base material and the cap material; and a lead frame. The lead frame further includes: a die pad on which the semiconductor chip is mounted; an inner lead portion sealed by the enclosure, the inner lead portion having a stacked structure in which a plurality of conductive layers are stacked via insulating layers, and the plurality of conductive layers are electrically connected to corresponding external connection electrodes on the semiconductor chip by bonding wires; and an outer lead portion leading out of the enclosure. Independent Claims 2 and 17 recite similar features in the context of a semiconductor device.

As explained from page 4, line 21 to page 5, line 6 of Applicant's specification, Applicant's invention improves upon background semiconductor devices, since it can provide a enclosure of a semiconductor chip with a magnetic shielding, for example to shield magnetic random access memories (MRAM) from magnetic fields.

Turning now to the applied art, the reference Butt, used by the outstanding Office Action as a primary reference to form the 35 U.S.C. §103(a) rejections, discloses a semiconductor package with a power device sealed therein, wherein a metal substrate 16 has a first surface 18 bonded to a second surface 20 of the cladding 14.[1] However, Butt fails to teach an inner lead portion sealed by the enclosure, the inner lead portion having a *stacked structure* in which a plurality of conductive layers are stacked via insulating layers, and *the plurality of conductive layers are electrically connected to corresponding external connection electrodes* on the semiconductor chip by bonding wires, as recited in amended independent Claims 1, 2 and 17. Butt explicitly teaches that the lead wires 25 from the power device 12 are attached to the leadframe 22.[2] Furthermore, Butt's Figure 4 shows that the lead wires are connected to individual terminal leads 60, which are arranged in parallel to each

[1] See Butt in the Abstract and at column 3, lines 57-61 and in corresponding Figure 1.
[2] See Butt for example at column 5, lines 24-26 and in corresponding Figure 1 and 3.

other.[3] Accordingly, wires 25 attached to a leadframe 22, as taught by Butt, ***are not*** a plurality of conductive layers being electrically connected to corresponding external connection electrodes, as claimed. Butt also fails to teach or suggest the claimed die pad on which the semiconductor chip is mounted, as recited in amended independent Claims 1, 2 and 17. Butt's power device 12 is mounted to a substrate 12 that is part of the enclosure of the semiconductor package.[4] This is done in order to "maximize the heat dissipation capability,"[5] as explained in Butt.

Both other references, Stobbs and Hirai, even if we assume *in arguendo* that the combination of these references is proper, fail to remedy the deficiencies of Butt, as next discussed.

Stobbs discloses a memory assembly including a substrate that incorporates magnetic shielding.[6] However, Stobbs is silent regarding the claimed features lead frame including a die pad and an inner lead portion having a stacked structure. Stobbs merely teaches that the inputs and outputs of an MRAM die may be electrically connected to one or more circuit pathways 18 printed or otherwise incorporated onto the substrate.[7] Accordingly, Stobbs fails to teach or suggest the inner lead portion having a stacked structure in which a plurality of conductive layers are stacked via insulating layers, and the plurality of conductive layers are electrically connected to corresponding external connection electrodes, as recited in amended Claims 1, 2 and 17.

The reference Hirai describes a MRAM memory structure for high-speed data read-out, wherein the memory elements includes a non-magnetic layer sandwiched between a hard layer made of magnetic material and a soft layer made of a magnetic material having a

[3] See Butt for example from column 5, line 67 to column 6, line 1 and in Figure 4.
[4] See Butt for example in Figures 1 and 3 and at column 5, lines 22-24.
[5] See Butt at column 5, lines 38-40.
[6] See Stobbs in the Abstract.
[7] See Stobbs at page 2, paragraph 20 and in Figures 2 and 3.

coercive force lower that the hard layer.[8] However, Hirai is entirely silent on any features regarding the enclosure of a semiconductor chip including a magnetic element. Hirai's teachings are related to the transistors for the MRAM memory itself, and therefore do not teach any of the features of independent Claims 1, 2 and 17.

Therefore, the applied references fail to teach or suggest every feature recited in Applicant's claims, so that Claims 1-7 and 12-20 are patentably distinct over the references of record. Accordingly, Applicant respectfully traverses, and requests reconsideration of, the rejections based on Butt, Stobbs and Hirai.[9]

Consequently, in view of the present amendment, no further issues are believed to be outstanding in the present application, and the present application is believed to be in condition for formal Allowance. A Notice of Allowance for Claims 1-7 and 12-20 is earnestly solicited.

Should the Examiner deem that any further action is necessary to place this application in even better form for allowance, the Examiner is encouraged to contact Applicant's undersigned representative at the below listed telephone number.

Respectfully submitted,

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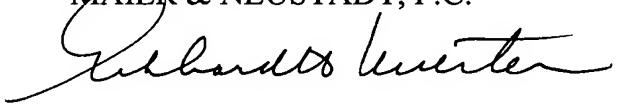

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[8] See Hirai in the Abstract, at page 1, paragraph 9 and in Figures 13-15.
[9] See MPEP 2131: "A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference," (Citations omitted) (emphasis added). See also MPEP 2143.03: "All words in a claim must be considered in judging the patentability of that claim against the prior art."